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| **PDP-8 ISA Simulator Project** |
| ECE 486 – Computer Architecture |
|  |
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# Project Overview

The purpose of this project is to simulate the PDP-8 Instruction Set Architecture. The PDP-8 ISA simulator should be capable of generating memory trace files.

**Inputs:**

The simulator should take either an ASCII or binary object code file. The input file will be produced by the PDP-8 Assembler provided.

**Outputs:**

After the completion of the execution, the simulator should generate a brief summary including:

* The total number of instructions executed.
* The total number of clock cycles consumed.
* The number of times each instruction type (by mnemonic) was executed.

In addition, the simulator must generate a trace file of all memory access (instruction and data) in order.

# Project Requirements

The following are requirements that need to be implemented into the project:

1. The simulator must correctly simulate the entire PDP-8 instruction set.
2. The simulator must be “clock accurate”.

# Design Specification and Implementation

**Information on PDP-8 Architecture:**

[FILL HERE]

**Instruction format and decoding:**

[FILL HERE]

**Addressing modes:**

[FILL HERE]

**Memory Module:**

[FILL HERE]

**Trace File Output Module:**

The format of the trace files will be as follows:

<type> <address>

Type:

0 - Data Read

1 - Data Write

2 - Instruction Fetch

Address:

The address should be displayed in octal.

**Interfacing between the different modules:**

[FILL HERE]

# Testing and Validation

To ensure all aspects of our module are operating correctly, we tested each of our modules and provided expected results and actual simulation results.

[REQ: Have a written test strategy]

**(Copy and paste the following format for each test case)**

**Testing and Validating “INSERT NAME HERE” Module:**

* Test Description:

Insert short description of what is being tested.

* Test Procedure:

Insert the procedure of how it will be tested.

* Expected and Simulated Results:

Insert the expected results followed by the simulated results.

# Cache Simulation Source Code

Name and attach respectively all source code files here.